REMARKS

Claim 13 and 14 are objected to. The claims are amended in a manner consistent with suggestions made in the Office Action. Reconsideration is requested.

Claims 1-46 and 49-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lowrey, *et al.* (U.S. Patent Number 6,813,177 - hereinafter Lowrey '177) in view of Tang, *et al.* (U.S. Patent Number 6,222,771) as supported by Ooishi (U.S. Patent Number 6,873,561). Claims 47 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lowrey '177 in view of Tang, *et al.* and further in view of Lowrey, *et al.* (U.S. Patent Number 6,608,773 - hereinafter Lowrey '773). In view of the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

In the present invention as claimed in claims 1-26, a method of programming a semiconductor memory device includes continuously applying a set pulse to the memory device. Applying the set pulse to the memory device includes applying a current to a bit line of the memory device. While the set pulse is applied, a state of the memory device is detected. When the memory device is determined to be in a desired set state, the set pulse is removed by removing the current applied to the bit line of the memory device, such that duration of the set pulse is controlled based on the state of the memory device.

In the present invention as claimed in claims 27-55, a semiconductor memory device includes a detecting circuit for detecting a state of the memory device and a controller for continuously applying a set pulse to the memory device by continuously applying a set current to a bit line of the memory device. The controller removes the set pulse when the memory device is detected to be in a desired set state, such that duration of the set pulse is controlled based on the state of the memory device.

Lowrey '177 discloses that a programming signal is applied to a memory cell and then removed. After the programming signal is removed, a resistance of the phase change material is read to determine if the memory cell was programmed to the desired state. If the memory cell was not programmed to the desired state, another program signal is applied and removed. This

process is repeated until the memory cell reaches the desired state.

Lowrey '177 fails to teach or suggest a method of programming a semiconductor memory device that includes, while a set pulse is applied to a memory device, a state of the memory device is detected, such that a duration of the set pulse is controlled based on the state of the memory device, as claimed in claims 1-26. Instead, in Lowrey '177, the programming signal is applied to the memory cell, and after the signal is applied and removed, it is determined whether the memory cell is in the desired state. Thus, the program signal is not applied while simultaneously detecting the state of the memory state as claimed in claims 1-26. Further, the duration of the program signal is not based on the state of the memory device as claimed in claims 1-26.

Further, Lowrey '177 fails to teach or suggest a semiconductor memory device includes a detecting circuit for detecting a state of the memory device and a controller for continuously applying a set pulse to the memory device by continuously applying a set current to a bit line of the memory device, the controller removing the set pulse when the memory device is detected to be in the desired set state, such that duration of the set pulse is controlled based on the state of the memory device, as set forth in amended claims 27-55. Instead, in Lowrey '177, the programming signal is applied to the memory cell, and after the signal is applied and removed, it is determined whether the memory cell is in the desired state, and, if it is not in the desired state, the signal is applied again. Thus, the program signal is not continuously applied and the duration of the program signal is not based on the state of the memory device, as claimed in claims 27-55.

Tang, *et al.* discloses a unified program method and circuitry for performing concurrently a program and verifying operation in a array of Flash EEPROM memory cells which eliminates the need of a current source. Thus, without applying a current to the memory device, there is no set pulse as claimed in claims 1-26 and 27-55.

Therefore, Tang, *et al.* fails to teach or suggest a method of programming a semiconductor memory device that includes, while a set pulse is applied to a memory device, a state of the memory device is detected, such that a duration of the set pulse is controlled based on the state of the memory device, as claimed in claims 1-26. Further, Tang, *et al.* fails to teach or suggest a semiconductor memory device includes a detecting circuit for detecting a state of the

memory device and a controller for continuously applying a set pulse to the memory device by continuously applying a set current to a bit line of the memory device, the controller removing the set pulse when the memory device is detected to be in the desired set state, such that duration of the set pulse is controlled based on the state of the memory device, as set forth in amended claims 27-55.

Ooishi is cited in the Office Action as disclosing a write enable feature. Ooishi fails to teach or suggest a method of programming a semiconductor memory device that includes, while a set pulse is applied to a memory device, a state of the memory device is detected, such that a duration of the set pulse is controlled based on the state of the memory device, as claimed in claims 1-26. Ooishi further fails to teach or suggest a semiconductor memory device includes a detecting circuit for detecting a state of the memory device and a controller for continuously applying a set pulse to the memory device by continuously applying a set current to a bit line of the memory device, the controller removing the set pulse when the memory device is detected to be in the desired set state, such that duration of the set pulse is controlled based on the state of the memory device, as set forth in amended claims 27-55.

Hence, none of Lowrey '177, Tang, *et al.* and Ooishi teaches or suggests certain elements of the present invention set forth in amended claims 1-26 and 27-55. Specifically, none of the references teaches or suggests a method of programming a semiconductor memory device that includes, while a set pulse is applied to a memory device, a state of the memory device is detected, such that a duration of the set pulse is controlled based on the state of the memory device, as claimed in claims 1-26. In addition, none of the references teaches or suggests a semiconductor memory device includes a detecting circuit for detecting a state of the memory device and a controller for continuously applying a set pulse to the memory device by continuously applying a set current to a bit line of the memory device, the controller removing the set pulse when the memory is detected to be in the desired set state, such that duration of the set pulse is controlled based on the state of the memory device, as set forth in amended claims 27-55. Accordingly, there is no combination of the references which would provide such teaching or suggestion.

None of the references, taken alone or in combination, teaches or suggests the invention

set forth in claims 1-26 and 27-55. Therefore, it is believed that the claims 1-46 and 49-55 are allowable over the cited references, and reconsideration of the rejections of claims 1-46 and 49-55 under 35 U.S.C. § 103(a) based on Lowrey '177, Tang, *et al.* and Ooishi is respectfully requested.

With regard to the rejection of claims 47 and 49, Lowrey '773 is cited in the Office Action as disclosing a set enable feature. Lowrey '773 fails to teach or suggest a method of programming a semiconductor memory device that includes, while a set pulse is applied to a memory device, a state of the memory device is detected, such that a duration of the set pulse is controlled based on the state of the memory device, as claimed in claims 1-26. Lowrey '773 further fails to teach or suggest a semiconductor memory device includes a detecting circuit for detecting a state of the memory device and a controller for continuously applying a set pulse to the memory device by continuously applying a set current to a bit line of the memory device, the controller removing the set pulse when the memory device is detected to be in the desired set state, such that duration of the set pulse is controlled based on the state of the memory device, as set forth in amended claims 27-55.

Hence, none of Lowrey '177, Tang, *et al.*, as discussed above, and Lowrey '773 teaches or suggests certain elements of the present invention set forth in amended claims 27-55. Specifically, none of the references teaches or suggests a semiconductor memory device includes a detecting circuit for detecting a state of the memory device and a controller for continuously applying a set pulse to the memory device by continuously applying a set current to a bit line of the memory device, the controller removing the set pulse when the memory device is detected to be in the desired set state, such that duration of the set pulse is controlled based on the state of the memory device, as set forth in amended claims 27-55. Accordingly, there is no combination of the references which would provide such teaching or suggestion.

None of the references, taken alone or in combination, teaches or suggests the invention set forth in claims 27-55. Therefore, it is believed that the claims 27-55 are allowable over the cited references, and reconsideration of the rejections of claims 47 and 48 under 35 U.S.C. § 103(a) based on Lowrey '177, Tang, *et al.* and Lowrey '773 is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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